What is claimed is:

1. A process comprising:

forming an electrically conductive seed film in a contact corridor in a first dielectric stack;

forming a stud electrode in the contact corridor, wherein the stud electrode is partially embedded in the contact corridor, and wherein the stud electrode is formed to extend from the first dielectric stack; and

electrically isolating the stud electrode.

2. The process according to claim 1, the process further including:

forming a storage cell plate over the stud electrode.

3. The process according to claim 1, wherein forming an electrically conductive seed film includes conformally forming the seed film upon sidewalls of the contact corridor.

4. The process according to claim 1, wherein the first dielectric stack includes an upper surface, and forming an electrically conductive seed film further includes:

conformally forming the seed film upon sidewalls of the contact corridor and upon the upper surface of the first dielectric stack.

5. The process according to claim 1, the contact corridor including a second dielectric stack during the process, after forming a stud electrode in the contact corridor, the process further including:

removing the second dielectric stack.

6. The process according to claim 1, wherein the first dielectric stack includes an upper surface, the process further including:

forming a protective film upon the upper surface of the first dielectric stack.

7. The process according to claim 1, wherein the first dielectric stack includes an upper surface, the process further including:

forming a protective film upon the upper surface of the first dielectric stack, and wherein electrically isolating the stud electrode includes etching at least a portion of the protective film.

8. The process according to claim 1, wherein electrically isolating the stud electrode includes:

forming a storage cell dielectric film over the stud electrode.

9. The process according to claim 1, the process further including:

forming a storage cell dielectric film over the stud electrode; and

forming a storage cell plate over the stud electrode.

10. The process according to claim 1, wherein forming a stud electrode is selected from through-hole electroplating, and through-hole electroless plating.

11. A process comprising:

forming a barrier structure above a first conductive plug;

forming a contact corridor to open at least a portion of the barrier structure;

forming an electrically conductive seed film in the contact corridor, wherein the seed film makes contact with the barrier structure;

forming a stud electrode in the contact corridor, wherein the stud electrode is partially embedded in the contact corridor, and wherein the stud electrode is formed to extend from the contact corridor; and

electrically isolating the stud electrode.

12. The process according to claim 11, forming a barrier structure above a first conductive plug further including:

forming a second conductive plug in a contact corridor, wherein the second conductive plug is above and on the first conductive plug;

saliciding a portion of the second conductive plug to form a first barrier film; and

forming a second barrier film above and on the first barrier film, wherein the second barrier film is selected from at least one of a nitride, a silicide, or a silicide-nitride of a refractory metal.

13. The process according to claim 11, forming a barrier structure over a first conductive landing pad further including:

etching back precursor polysilicon material to form the first conductive plug; and

forming a silicide first barrier film above the first conductive plug.

14. The process according to claim 11, forming a barrier structure over a first conductive plug further including:

etching back precursor polysilicon material to form the first conductive ; and

forming a silicide first barrier film above the first conductive plug, wherein forming a silicide first barrier film includes depositing by a process selected from CVD, PVD, and ALD, and wherein the silicide first barrier film includes saliciding a metal film.

15. The process according to claim 11, forming a barrier structure over a first conductive plug further including:

etching back precursor polysilicon material to form the first conductive plug;

forming a silicide first barrier film above the first conductive plug; and

forming a second barrier film above the first barrier film.

16. The process according to claim 11, forming a barrier structure over a first conductive plug further including:

forming a precursor polysilicon material above a substrate;

etching back the precursor polysilicon material to form the first conductive plug;

forming a silicide first barrier film above the first conductive plug; and

forming a second barrier film above the first barrier film, wherein the second barrier film is formed by a process selected from CVD, PVD, and ALD, and wherein the second barrier film includes a film selected from a refractory metal nitride a refractory metal silicide, and a refractory metal silicide-nitride.

17. The process according to claim 11, forming a barrier structure over a first conductive plug further including:

forming a precursor polysilicon material above a substrate;

etching back the precursor polysilicon material to form the first conductive plug;

forming a silicide first barrier film above the first conductive plug;

forming a second barrier film above the first barrier film; and

planarizing the second barrier film to form an upper surface.

18. A process of forming a stud capacitor structure, comprising:

forming a precursor polysilicon material above a substrate;

etching back the precursor polysilicon material to form a first conductive plug;

forming a barrier structure above the first conductive plug, wherein the barrier structure includes a salicide first barrier film and a refractory metal compound second barrier film;

forming a seed film in a recess that opens to the barrier structure, wherein the seed film includes a metal selected from platinum, ruthenium, iridium, palladium, nickel, combinations thereof, and an alloy;

forming a stud electrode in the recess to embed a portion thereof in the recess, and to cause another portion thereof to extend from the recess;

forming a dielectric film over the stud electrode; and

forming a storage cell plate over the dielectric film.

19. The process of forming a stud capacitor structure according to claim 18, wherein forming the barrier structure includes:

opening a contact corridor above the first conductive plug;

forming a second conductive plug above and on the first conductive plug; and

depositing the barrier structure into the contact corridor.

20. The process of forming a stud capacitor structure according to claim 18, wherein forming the barrier structure includes:

saliciding the first conductive plug.

21. The process of forming a stud capacitor structure according to claim 18, wherein forming the barrier structure includes:

saliciding the first conductive plug; and

forming a refractory metal nitride barrier film above the first conductive plug.

22. A stud capacitor structure comprising:

a first conductive plug disposed above a substrate;

a stud coupled to the first conductive plug, wherein the stud is partially embedded in a first dielectric stack; and

an upper dielectric stack disposed above the first dielectric stack, wherein the stud extends into the upper dielectric stack.

23. The stud capacitor structure according to claim 22, the structure further including:

a seed film disposed above the first conductive plug, wherein the seed film is below and on the stud.

24. The stud capacitor structure according to claim 22, the structure further including:

a seed film disposed above the first conductive plug, wherein the seed film is below and on the stud, and wherein the seed film is embedded in the first dielectric stack.

25. The stud capacitor structure according to claim 22, the structure further including:

a storage cell dielectric film disposed over the stud; and

a storage cell plate disposed over the storage cell dielectric film.

26. The stud capacitor structure according to claim 22, the structure further including:

a storage cell dielectric film disposed over the stud, wherein the storage cell dielectric film has a thickness in a range from about 30 Å to about 80 Å.

27. The stud capacitor structure according to claim 22, the structure further including:

a storage cell dielectric film disposed over the stud, wherein the storage cell dielectric film is selected from titanium oxide, tantalum oxide, aluminum oxide, strontium titanate, barium strontium titanate, lead titanate, lead lanthanum titanate, lead lanthanum zirconium tantalate, lead zirconium titanate, strontium bismuth tantalate, and combinations thereof.

28. The stud capacitor structure according to claim 22, the structure further including:

a storage cell dielectric film disposed over the stud, wherein the storage cell dielectric film has a dielectric constant range from about 9 to about 300; and

a storage cell plate disposed over the storage cell dielectric film.

29. The stud capacitor structure according to claim 22, the structure further including:

a storage cell dielectric film disposed over the stud; and

a storage cell plate disposed over the storage cell dielectric film, wherein the storage cell plate is selected from the same material as the stud, platinum, rhodium, ruthenium, iridium, palladium, nickel, combinations thereof, and an alloy.

30. The stud capacitor structure according to claim 22, the structure further including:

a storage cell dielectric film disposed over the stud; and

a storage cell plate disposed over the storage cell dielectric film, wherein the storage cell plate is a different material from the stud, selected from a metal nitride, titanium nitride, tantalum nitride, and tungsten nitride.

31. The stud capacitor structure according to claim 22, the structure further including:

a barrier structure disposed between and in contact with the stud above and the first conductive plug below.

32. The stud capacitor structure according to claim 22, the structure further including:

a barrier structure disposed between and in contact with the stud above and the first conductive plug below, wherein the barrier structure is disposed above a polysilicon plug.

33. The stud capacitor structure according to claim 22, the structure further including:

a barrier structure disposed between and in contact with the stud above and the first conductive plug below, wherein the barrier structure is disposed above a tungsten plug.

34. The stud capacitor structure according to claim 22, the structure further including:

a barrier structure disposed between and in contact with the stud above and the first conductive plug below, wherein the barrier structure is disposed above and on the first conductive plug.

35. A storage cell comprising:

a platinum stud partially embedded in a first dielectric stack, wherein the platinum stud is above and on a platinum seed film;

a first conductive plug disposed below the platinum seed film;

a barrier structure disposed between the platinum seed film and the first conductive plug;

a tantalum oxide dielectric film disposed over the platinum stud; and

a platinum cell plate disposed over the tantalum oxide dielectric film.

36. The storage cell according to claim 35, wherein the barrier structure further includes:

a metal silicide first barrier film disposed above and on the first conductive plug; and

a refractory metal nitride second barrier film disposed above and on the metalsilicide first barrier film.

37. The storage cell according to claim 35, wherein the barrier structure is disposed above and on a polysilicon first conductive plug.

38. The storage cell according to claim 35, wherein the barrier structure is disposed above and on a tungsten first conductive plug.

39. The storage cell according to claim 35, wherein the barrier structure is disposed above and on the first conductive plug, wherein the first conductive plug is selected from polysilicon and tungsten.

40. The storage cell according to claim 35, wherein the tantalum oxide dielectric film has a thickness in a range from about 30 Å to about 80 Å.

41. An electrical device comprising:

a storage cell stud partially embedded in a first dielectric stack, wherein the storage cell stud extends into an upper dielectric stack that is disposed above and on the first dielectric stack;

a seed film disposed against the storage cell stud, wherein the seed film is disposed in a contact corridor in the first dielectric stack; and

a protective film remnant disposed on an upper surface of the first dielectric stack, wherein the protective film remnant is disposed between the first dielectric stack and a portion of the seed film.

42. The electrical device according to claim 41, the electrical device further including:

a storage cell dielectric film disposed above the storage cell stud; and

a storage cell plate disposed above the storage cell dielectric film.

43. The electrical device according to claim 41, the electrical device further including:

a storage cell dielectric film disposed above the storage cell stud, wherein the storage cell dielectric film has a thickness in a range from about 30 Å to about 80 Å; and

a storage cell plate disposed above the storage cell dielectric film.

44. The electrical device according to claim 41, the electrical device further including:

a storage cell dielectric film disposed above the storage cell stud, wherein the storage cell dielectric film has a dielectric constant range from about 9 to about 300; and

a storage cell plate disposed above the storage cell dielectric film.

45. The electrical device according to claim 41, wherein the electrical device further includes:

a chip package, wherein the storage cell stud is disposed in the chip package.

46. The electrical device according to claim 41, wherein the electrical device further includes:

a chip package, wherein the storage cell stud is disposed in the chip package; and

a host, wherein the chip package is disposed in the host.

47. The electrical device according to claim 41, wherein the electrical device further includes:

a chip package, wherein the storage cell stud is disposed in the chip package; and

a host, wherein the chip package is disposed in the host, wherein the host includes a memory module.

48. The electrical device according to claim 41, wherein the electrical device further includes:

a chip package, wherein the storage cell stud is disposed in the chip package; and

a host, wherein the chip package is disposed in the host, wherein the host includes a memory module; and

an electronic system, wherein the memory module is disposed in the electronic system.

49. The electrical device according to claim 41, wherein the electrical device further includes:

a chip package, wherein the storage cell stud is disposed in the chip package;

a host, wherein the chip package is disposed in the host, wherein the host includes a dynamic random access memory module; and

an electronic system, wherein the dynamic random access memory module is disposed in the electronic system.

50. The electrical device according to claim 41, wherein the electrical device further includes:

a chip package, wherein the storage cell stud is disposed in the chip package;

a host, wherein the chip package is disposed in the host; and

an electronic system, wherein the host is disposed in the electronic system.

51. An electronic system, comprising:

a circuit module;

a user interface; and

a stud capacitor structure disposed in the circuit module or the user interface, the storage cell stud including:

a first conductive plug disposed above a substrate;

a stud coupled to the first conductive plug, wherein the stud is partially embedded in a first dielectric stack; and

an upper dielectric stack disposed above the first dielectric stack, wherein the stud extends into the upper dielectric stack.

52. The electronic system according to claim 51, wherein the user interface includes at least one of a keyboard, a pointing device, a monitor, a printer, a tuning dial, a display and speakers of a radio, an automobile ignition switch, an automobile gas pedal, a card reader, a keypad, and an automated teller machine.

53. The electronic system according to claim 51, wherein the circuit module includes a single integrated circuit.

54. A memory system, comprising:

a memory device;

a memory controller;

an external system bus; and

a command link; and

a stud capacitor structure disposed in the circuit module or the user interface, the storage cell stud including:

a first conductive plug disposed above a substrate;

a stud coupled to the first conductive plug, wherein the stud is partially embedded in a first dielectric stack; and

an upper dielectric stack disposed above the first dielectric stack, wherein the stud extends into the upper dielectric stack.

55. The memory system according to claim 54, wherein the memory system is selected from one of DIMM DRAM, a SIMM DRAM, a DIMM SDRAM, a SIMM SDRAM, a DIMM DDRAM, and a SIMM DDRAM.

56. A computer system, comprising:

a processor;

a memory system coupled to the processor;

an input/output (I/O) circuit coupled to the processor and the memory system; and

a stud capacitor structure disposed in the processor or the memory system, the storage cell stud including:

a first conductive plug disposed above a substrate;

a stud coupled to the first conductive plug, wherein the stud is partially embedded in a first dielectric stack; and

an upper dielectric stack disposed above the first dielectric stack, wherein the stud extends into the upper dielectric stack.

57. The computer system according to claim 56, wherein the processor is disposed in a host selected from a clock, a television, a cell phone, a personal computer, an automobile, an industrial control system, an aircraft, and a hand-held.

58. The computer system according to claim 56, wherein the memory system is selected from a DIMM DRAM, a SIMM DRAM, a DIMM SDRAM, a SIMM SDRAM, a DIMM DDRAM, and a SIMM DDRAM, and wherein the computer system is selected from a personal computer, a server, and a network computer.